L26-DR Series
Hardware Design

GNSS Products

Version: 1.7

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Status: Released

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The following safety precautions must be observed during all phases of operation, such as usage, service, or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all product manuals. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Ensure that the product may be used in the country and the required environment, as well as that it conforms to the local safety and environmental regulations.
	Keep away from explosive and flammable materials. The use of electronic products in extreme power supply conditions and locations with potentially explosive atmospheres may cause fire and explosion accidents.
	The product must be powered by a stable voltage source, and the wiring shall conform to security precautions and fire prevention regulations.
	Proper ESD handling procedures must be followed throughout the mounting, handling and operation of any devices and equipment that incorporate the module to avoid ESD damages.

About the Document

Document Information	
Title	**L26-DR Series Hardware Design**
Subtitle	GNSS Products
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Revision History

Version	Date	Description
-	2019-04-28	Creation of the document
1.0	2019-04-28	First official release
1.1	2019-10-19	1. Updated RF path in Figure 1; 2. Updated Chapter 2.1; 3. Updated power consumption in Table 1; 4. Updated the comment of CAN, FWD, WHEELTICK interfaces in Table 4; 5. Added TVS diode model in Figure 3; 6. Updated the update rate in Table 5; 7. Updated Chapter 3.5; 8. Added reference document for RF layout guide in Chapter 4; 9. Modified the description for recommended antenna specifications; 10. Deleted the reference design for external LNA and relevant description; 11. Updated Figure 4, 14, 15 and 16; 12. Updated Table 13; 13. Modified the description for module mounting and added content about the installation of L26-DR (UDR) Chapter 6.4.
1.2	2021-06-02	1. Changed the name of PIN1 from WAKE_UP to WAKEUP; 2. Changed the name of PIN3 from TIMEPULSE to 1PPS; 3. Changed the name of PIN9 from VCC_RF to VDD_RF;

Version	Date	Description
		4. Changed the names of PIN16 and PIN17 from ANT2 to ANT_DET2, ANT1 to ANT_DET1; 5. Changed the names of PIN18 and PIN19 from CANTX to CAN_TX, CANRX to CAN_RX; 6. Changed the names of PIN20 and PIN21 from UART_TX to TXD, UART_RX to RXD; 7. Chapter 1.2: Updated the Table 2; 8. Chapter 1.5: Added the description of GNSS constellations; 9. Chapter 3.3.2: Updated the description of standby mode; 10. Chapter 3.3.3, 3.4 and 3.5: Added these sections; 11. Chapter 4.1.1: Updated the description of UART; 12. Chapter 4.2.2: Updated the description of BOOT; 13. Chapter 5.2.3.1: Update the description of active antenna reference design; 14. Chapter 5.3: Added this section; 15. Chapter 6.2: Updated the description of operating conditions; 16. Chapter 8.2: Updated the notes about module storage; 17. Chapter 8.3: Updated the recommended peak reflow temperature and the reflow time in reflow zone; 18. Chapter 9: Added this chapter.
1.3	2021-06-28	1. Changed the grade of L26-DR(ADR) from industrial to automotive; 2. Deleted the L26-DR(ADRA), and added the L26-DR(ADRC); 3. Modified the 6-axis MEMS sensor to 6-axis IMU; 4. Updated the Table 2; 5. Updated the Table 3; 6. Modified the titles (Chapter 6.2); 7. Added sequence figures of entering/exiting the standby mode and backup mode (Figure 7 and Figure 8); 8. Added the power supply rating of RESET_N pin (Table 10); 9. Updated the description of RESET_N pin (Chapter 4.2.1).
1.4	2022-05-24	1. Updated descriptions of WAKEUP, WHEELTICK, BOOT, ANT_ON, FWD, TXD, RXD, and V_BCKP pins (pins 1, 4, 6, 14, 15, 20, 21, and 22); 2. Updated key features, product features, product performance, block diagram, descriptions of QZSS, SBAS, and AGNSS, and added information about firmware upgrade (Chapter 1); 3. Updated the reference charging circuit with rechargeable backup battery and added notes (Chapter 3.2.2); 4. Added the chapter of Feature Comparison (Chapter 3.3.1); 5. Updated ways to exit the Standby mode (Chapter 3.3.3); 6. Updated details of the Backup mode (Chapter 3.3.4); 7. Updated details of power-up sequence (Chapter 3.4);

Version	Date	Description
		8. Updated details of power-down sequence (Chapter 3.5); 9. Updated details of UART and CAN bus interfaces, added the chapter of ANT_DET1 and ANT_DET2, and updated information about WI and 1PPS (Chapter 4.1); 10. Updated the note on RESET_N (Chapter 4.2.2); 11. Updated the antenna selection guide (Chapter 5.1.2); 12. Updated recommended footprint figure (Figure 22); 13. Updated absolute maximum ratings of VCC and V_BCKP, added typical voltages of CAN_TX and CAN_RX, updated minimum and maximum voltages of WAKEUP, added details of supply current requirement, and updated information on ESD protection (Chapter 6); 14. Updated packaging information of the module (Chapter 8.1); 15. Updated the max slope of reflow zone and added notes on ultrasonic technology and SMT process (Chapter 8.3).
1.5	2023-06-30	1. Added the applicable variant L26-DR (AA). 2. Added the number of concurrent GNSS of L26-DR (ADR, UDR, ADRC) (*Table 2*). 3. Updated the tolerances for length and width of L26-DR (ADR, UDR, ADRC) (*Table 2* and *Figure 21*). 4. Added the power data, and updated the accuracy of 1PPS signal for L26-DR (ADR, UDR, ADRC) (*Table 3*). 5. Updated the power consumption of acquisition and tracking for L26-DR (ADR, ADRC) (*Table 3*, *Table 11* and *Table 12*). 6. Updated the pins 18 and 19 from CAN_RX and CAN_TX to RESERVED for L26-DR (ADRC) (*Chapters 2* and *4.1.1*). 7. Added the note of WHEELTICK and FWD for L26-DR (ADR, ADRC) (*Chapters 2*, *4.1.2*, and *4.1.3*). 8. Added the DC characteristics of all pins (*Table 6*). 9. Deleted the rechargeable battery circuit and added the 3.7 V lithium battery reference circuit (*Chapter 3.2.2*). 10. Specified the software commands for entering/exiting Standby mode (*Chapter 3.3.3*). 11. Specified the software commands for entering/exiting Backup mode and added the time requirement for entering the Backup mode (*Chapter 3.3.4*). 12. Added the note of CAN bus interface for L26-DR (ADR) (*Chapter 4.1.1*). 13. Added the chapter of avoiding current leakage on I/O pins (*Chapter 4.3*). 14. Updated the passive antenna gain and active antenna noise figure (*Table 9*). 15. Added the optional SAW filter circuit to active and passive antenna reference designs, as well as the corresponding description (*Chapter 5.2*).

Version	Date	Description
		16. Updated the maximum input power at RF_IN for L26-DR (ADR, UDR, ADRC) (*Table 10*). 17. Added the high-level input voltage range of RESET_N and the maximum output current of VDD_RF, and updated the output voltage of VDD_RF for L26-DR (ADR, UDR, ADRC). 18. Added the module mounting direction (*Chapter 8.1.3*). 19. Added the sizes of pizza box and carton (*Chapter 8.1.4*). 20. Updated the recommended ramp-to-soak, ramp-up and cool-down slopes (*Figure 28* and *Table 15*).
1.6	2024-11-25	1. Reserved the following pins: ● Reserved pins CAN_RX and CAN_TX (pins 18 and 19) for L26-DR (ADR) (*Chapters 1.1*, *1.2*, *2 and 4.1.1*). ● Reserved pin WI (pin 2) for L26-DR (ADRC, UDR) (*Chapters 2* and *4.1.4*). 2. Updated the dimensional tolerances for height and width (*Table 2* and *Figure 21*). 3. Updated product performance (*Table 3*): ● Updated test conditions for power consumption, TTFF (without AGNSS), accuracy of 1PPS signal, velocity accuracy, acceleration accuracy and dynamic performance. ● Deleted the 3σ accuracy of 1PPS signal. 4. Updated the note about connection requirement for WHEELTICK and FWD pins for L26-DR (ADR, ADRC) (*Chapters 2*, *4.1.2* and *4.1.3*). 5. Moved information related to antenna selection guide and coexistence with cellular systems to Quectel_GNSS_Antenna_Application_Note. 6. Added the axial ratio, -3 dB beam width and out-of-band rejection of active antenna (*Table 9*). 7. Added the note on the measured supply current values (*Chapter 6.2*). 8. Updated the module coplanarity requirement (*Chapter 7.1*). 9. Updated the recommended mounting for L26-DR (ADRC) (*Chapter 7.3*). 10. Updated the pizza box size (*Chapter 8.1*). 11. Updated manufacturing and soldering related information (*Chapter 8.3*): ● Updated the reference document for recommended module stencil thickness. ● Added the note specifying that mercury-containing materials should be avoided for module processing. ● Added the note prohibiting storage or use of unprotected modules in environments containing corrosive gases.
1.7	2025-08-27	1. Updated the storage temperature range (*Table 2* and *Table 10*). 2. Added the DR position error (ADR) for L26-DR (ADR, ADRC) (*Table 3*). 3. Added a note about module operating voltage range (*Chapter 2*). 4. Updated active antenna noise figure (*Table 9*).

Version	Date	Description
		5. Deleted the chapter of recommended operating conditions (*Chapter 6*). 6. Updated the pre-baking time to 24 h (*Chapter 8.2*).

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Table Index

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1 Product Description

1.1. Overview

Quectel L26-DR series module supports multiple global positioning and navigation systems: GPS, GLONASS, Galileo, BDS, and QZSS. The module also supports SBAS (including WAAS, EGNOS, MSAS, and GAGAN) and AGNSS functions. The L26-DR series comprises four variants: L26-DR (AA), L26-DR (ADR), L26-DR (ADRC), and L26-DR (UDR).

Key features:

- Single-band, multi-constellation GNSS modules that feature a high-performance, high-reliability positioning engine facilitating fast and precise GNSS positioning.
- The L26-DR (ADR, UDR, ADRC) have a 6-axis integrated IMU to support the Dead Reckoning (DR) feature.
- Supported serial communication interface: UART.
- The automotive-grade variants L26-DR (ADR, ADRC) support Automotive Dead Reckoning (ADR) technology. They achieve continuous and accurate vehicle positioning by combining GNSS and 6-axis IMU data and speed information from the vehicle.
- L26-DR (ADR) applies to 4-wheeled vehicles and L26-DR (ADRC) applies to 2-wheeled vehicles.
- The industrial-grade variant L26-DR (UDR) supports Untethered Dead Reckoning (UDR) technology and, without requiring speed information from the vehicle, uses only GNSS and 6-axis IMU data to achieve continuous and accurate vehicle positioning.
- The integrated flash memory provides the capacity for storing user-specific configurations and future firmware upgrades.

The L26-DR is a series of SMD type modules with a compact form factor of 12.2 mm × 16.0 mm × 2.3 mm. It can be embedded in your applications through 24 LCC pins.

The module is fully compliant with the EU RoHS Directive.

NOTE

Where applicable, this document will use the words module/modules when referring to common attributes, and "L26-DR (AA)", "L26-DR (ADR)", "L26-DR (UDR)", and "L26-DR (ADRC)" when referring to attributes associated with a particular subset of module.

1.1.1. Special Mark

Table 1: Special Mark

Mark	Definition
●	The symbol indicates that a function or technology is supported by the module(s).

1.2. Features

Table 2: Product Features

Features		L26-DR (AA)	L26-DR (ADR)	L26-DR (UDR)	L26-DR (ADRC)
Grade	Industrial	-	-	●	-
	Automotive	●	●	-	●
Category	Standard Precision GNSS	●	●	●	●
	High Precision GNSS	-	-	-	-
	DR	-	●	●	●
	RTK	-	-	-	-
	Timing	-	-	-	-
VCC Voltage	3.0–3.6 V, Typ. 3.3 V	●	●	●	●
V_BCKP Voltage	2.0–3.6 V, Typ. 3.3 V	●	●	●	●
I/O Voltage	Following VCC	●	●	●	●
Communication Interfaces	UART	●	●	●	●
	SPI	-	-	-	-
	I2C	-	-	-	-
	CAN	-	-	-	-
	USB	-	-	-	-
Integrated	Additional LNA	●	●	●	●

Features			L26-DR (AA)	L26-DR (ADR)	L26-DR (UDR)	L26-DR (ADRC)
Features	Additional Filter		●	●	●	●
	RTC Crystal		●	●	●	●
	TCXO Oscillator		●	●	●	●
	6-axis IMU		-	●	●	●
Constellations and Frequency Bands	Number of Concurrent Constellations		3 + QZSS	3 + QZSS	3 + QZSS	3 + QZSS
	GPS	L1 C/A	●	●	●	●
		L2C	-	-	-	-
		L5	-	-	-	-
	GLONASS	L1	●	●	●	●
		L2	-	-	-	-
	Galileo	E1	●	●	●	●
		E5a	-	-	-	-
		E5b	-	-	-	-
	BDS	B1I	●	●	●	●
		B1C	-	-	-	-
		B2a	-	-	-	-
		B2I	-	-	-	-
	QZSS	L1 C/A	●	●	●	●
		L2C	-	-	-	-
		L5	-	-	-	-
	NavIC	L5	-	-	-	-
	SBAS	L1	●	●	●	●
Temperature Range	Operating temperature range: -40 °C to +85 °C Storage temperature range: -40 °C to +95 °C					
Physical Characteristics	Size: (12.2 +0.3/-0.15) mm × (16.0 +0.3/-0.15) mm × (2.3 ±0.20) mm Weight: Approx. 0.9 g					

NOTE

For more information about GNSS constellation configuration, see *document [1] protocol specification*.

1.3. Performance

Table 3: Product Performance

Parameter	Specification	L26-DR (AA)	L26-DR (ADR)	L26-DR (UDR)	L26-DR (ADRC)
Power Consumption [1]	Acquisition	G3 [2] + QZSS 81 mA (267.3 mW)	G3 [2] 81 mA (267.3 mW)	G3 [2] 84 mA (277.2 mW)	G3 [2] + QZSS 81 mA (267.3 mW)
	Tracking	81 mA (267.3 mW)	80 mA (264 mW)	81 mA (267.3 mW)	80 mA (264 mW)
	Standby mode [3]	1.7 mA (5.61 mW)	1.7 mA (5.61 mW)	1.7 mA (5.61 mW)	1.7 mA (5.61 mW)
	Backup mode	8 μA (26.4 μW)	8 μA (26.4 μW)	8 μA (26.4 μW)	8 μA (26.4 μW)
Sensitivity (GPS + GLONASS)	Acquisition	-145 dBm	-145 dBm	-145 dBm	-145 dBm
	Reacquisition	-152 dBm	-152 dBm	-152 dBm	-152 dBm
	Tracking	-162 dBm	-162 dBm	-162 dBm	-162 dBm
TTFF [1] (without AGNSS)	Cold Start	32 s	32 s	32 s	32 s
	Warm Start	27 s	25 s	25 s	25 s
	Hot Start	2 s	2 s	2 s	2 s
TTFF [4] (with AGNSS)	Cold Start	13 s	13 s	13 s	13 s
DR Position Error (ADR)	4-wheeler (Without GNSS)	-	< 2 % of distance traveled	-	-
	2-wheeler (Without GNSS)	-	-	-	< 2 % of distance traveled

[1] Tested at room temperature, with typical operating voltage, and satellites signal of -130 dBm configured by the instrument.
[2] G3 is GPS + GLONASS + Galileo.
[3] Total power consumption of the module in the Standby mode.
[4] Open-sky, active high-precision GNSS antenna.

Parameter	Specification	L26-DR (AA)	L26-DR (ADR)	L26-DR (UDR)	L26-DR (ADRC)
Horizontal Position Accuracy [5]		1.5 m	1.5 m	1.5 m	1.5 m
Update Rate		1 Hz (Max. 10 Hz)	1 Hz	1 Hz (Max. 10 Hz)	1 Hz (Max. 10 Hz)
Accuracy of 1PPS Signal [1]	RMS	50 ns	32 ns	44 ns	45 ns
Velocity Accuracy [1]	Without Aid	0.1 m/s	0.1 m/s	0.1 m/s	0.1 m/s
Acceleration Accuracy [1]	Without Aid	0.1 m/s²	0.1 m/s²	0.1 m/s²	0.1 m/s²
Dynamic Performance [1]	Max. Altitude	18000 m	18000 m	18000 m	18000 m
	Max. Velocity	515 m/s	515 m/s	515 m/s	515 m/s
	Max. Acceleration	4g	4g	4g	4g

1.4. Block Diagram

A block diagram of the modules is presented below. It includes a front-end section with an additional LNA and two SAW filters, a TCXO, an LDO, a load switch, an XTAL, a GNSS IC with a PMU and a 6-axis IMU (not supported by L26-DR (AA)). The first SAW filter improves out-of-band rejection. Consequently, the LNA will be less likely to produce in-band interference in challenging environments, which ensures enhanced performance in a jamming environment.

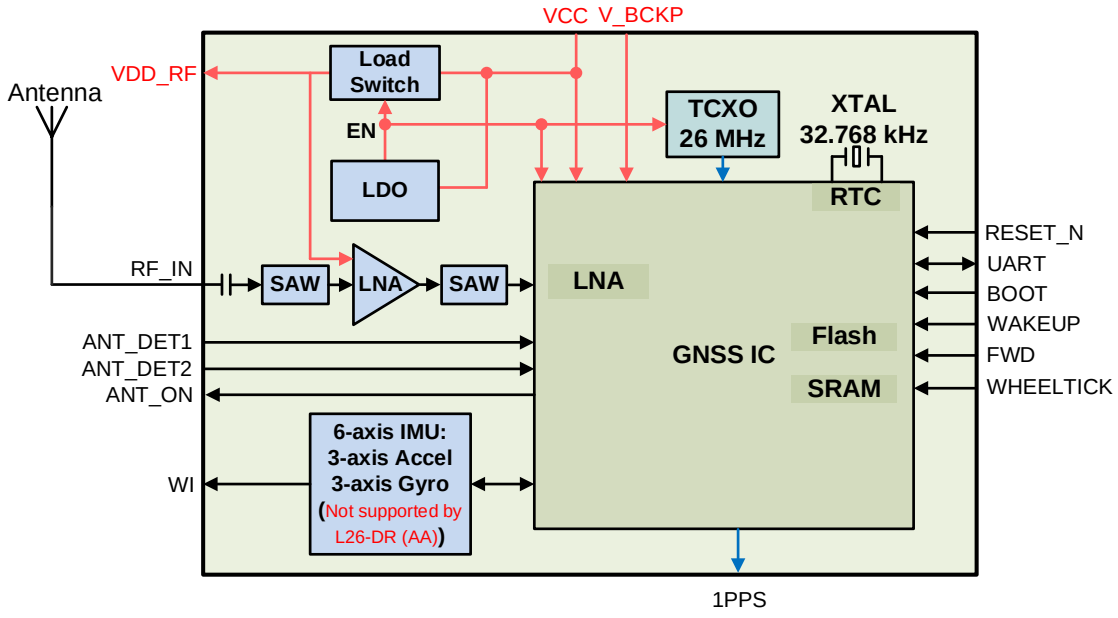


Figure 1: Block Diagram

[5] CEP 50 %, 24 hours static, -130 dBm, more than 6 SVs.

NOTE

1. The 6-axis IMU is not supported by L26-DR (AA).
2. The WI pin is only supported by L26-DR (ADR).
3. The WHEELTICK and FWD pins are only supported by L26-DR (ADR, ADRC).

1.5. GNSS Constellations and Frequency Bands

The module is a single-band concurrent GNSS receiver that can receive and track multiple GNSS signals. Owing to its RF front-end architecture, it can track the following GNSS constellations: GPS, GLONASS, Galileo, BDS, and QZSS, plus SBAS satellites. If low power consumption is a key factor, then the module can be configured for a subset of GNSS constellations.

QZSS is a regional navigation satellite system that transmits signals compatible with the GPS L1 C/A, L1C, L2C and L5 signals for the Pacific region covering Japan and Australia. The module can detect and track QZSS L1 C/A signal concurrently with GPS signals, leading to better availability especially under challenging conditions, e.g., in urban canyons.

Table 4: GNSS Constellations and Frequency Bands

System	Signal
GPS	L1 C/A: 1575.42 MHz
GLONASS	L1: 1602 MHz + K × 562.5 kHz, K= (-7 to +6, integer)
Galileo	E1: 1575.42 MHz
BDS	B1I: 1561.098 MHz
QZSS	L1 C/A: 1575.42 MHz

1.6. Augmentation System

1.6.1. SBAS

The module supports SBAS signal reception. By augmenting primary GNSS constellations with additional satellite-broadcast messages, the system improves the accuracy and reliability of GNSS information by correcting signal measurement errors and providing information about signal accuracy, integrity, continuity, and availability. SBAS transmits signals for ranging or distance measurement, thus further improving availability. Supported SBAS systems: WAAS, EGNOS, MSAS and GAGAN.

1.7. AGNSS

The module supports the AGNSS feature that significantly reduces its TTFF, especially under lower signal conditions. To implement the AGNSS feature, the module should get the assistance data including the current time and rough position. For more information, see *document [2] AGNSS application note*.

1.8. Dead Reckoning Function

The L26-DR (ADR, UDR, ADRC) support the Dead Reckoning (DR), which is the process of estimating the module's current position based on the last position obtained from GNSS, speed, heading sensor data, etc. With the combined 6-axis IMU data input, the software system can continuously update the positioning coordinates when the GNSS satellite signals are partially or completely blocked, while GNSS satellite signals provide updates and corrections for the 6-axis IMU drift. With this technology, the system achieves continuous and high-accuracy positioning in environments such as tunnels and urban canyons. For more information about DR function, see *documents [3]* and *[4] DR application notes*.

1.9. Firmware Upgrade

The module is delivered with preprogrammed firmware. Quectel may release firmware versions that contain bug fixes or performance optimizations. It is highly important to implement a firmware upgrade mechanism in your system. A firmware upgrade is the process of transferring a binary file image to the receiver and storing it in non-volatile flash. For more information, see *document [5] firmware upgrade guide*.

2 Pin Assignment

The module is equipped with 24 LCC pins by which the module can be mounted on your PCB.

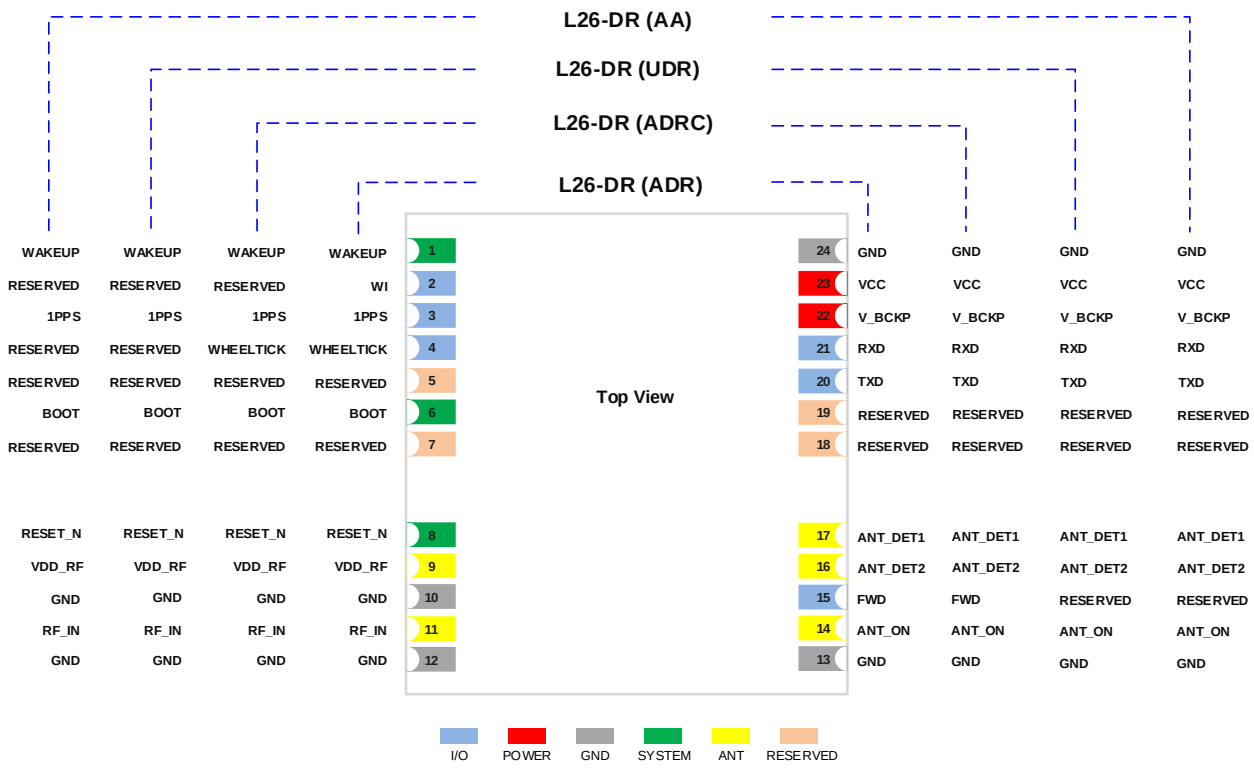


Figure 2: Pin Assignment

NOTE

When using the Wheel Tick Mode to obtain speed information, ensure that the WHEELTICK and FWD pins are connected on L26-DR (ADR, ADRC).

Table 5: I/O Parameter Definition

Type	Description
AI	Analog Input
DI	Digital Input

Type	Description
DO	Digital Output
PI	Power Input
PO	Power Output

Table 6: Pin Description

Function	Name	No.	I/O	Description	DC Characteristics	Remarks
Power	VCC	23	PI	Main power supply	$V_I$min = 3.0 V $V_I$nom = 3.3 V $V_I$max = 3.6 V	Requires clean and steady voltage.
	V_BCKP	22	PI	Backup power supply for backup domain	$V_I$min = 2.0 V $V_I$nom = 3.3 V $V_I$max = 3.6 V	V_BCKP must be connected to power supply for startup, and it should always be powered if hot (warm) start is needed.
I/O	TXD	20	DO	Transmits data	V_{OL}max = 0.4 V V_{OH}min = VCC - 0.4 V	UART interface supports standard NMEA messages, PSTM messages, speed information (not supported by L26-DR (AA, UDR)) and firmware upgrade.
	RXD	21	DI	Receives data	V_{IL}min = -0.3 V V_{IL}max = 0.8 V V_{IH}min = 2.0 V V_{IH}max = VCC + 0.3 V	
	FWD	15	DI	Forward/backward status signal input	V_{IL}min = -0.3 V V_{IL}max = 0.8 V V_{IH}min = 2.0 V V_{IH}max = VCC + 0.3 V	Pulled up internally by default. L26-DR (AA, UDR) do not support the functions. If unused, leave the pins N/C (not connected).
	WHEELTICK	4	DI	Odometer/wheel-tick pulse input	V_{IL}min = -0.3 V V_{IL}max = 0.8 V V_{IH}min = 2.0 V V_{IH}max = VCC + 0.3 V	
	WI	2	DO	Warning indicator	V_{OL}max = 0.4 V V_{OH}min = VCC - 0.4 V	VCC must be valid to ensure the interrupt signal output. L26-DR (AA, ADRC, UDR) do not support the function.

Function	Name	No.	I/O	Description	DC Characteristics	Remarks
						If unused, leave the pins N/C.
	1PPS	3	DO	One pulse per second	V_{OL}max = 0.4 V V_{OH}min = VCC - 0.4 V	Synchronized on the rising edge. If unused, leave the pin N/C.
ANT	VDD_RF	9	PO	Power supply for external RF components	$V_O$nom = VCC	VDD_RF = VCC, the output current capacity depends on VCC. Typically used to supply power for an external active antenna or LNA. In the Backup mode, VDD_RF is turned off. If unused, leave the pin N/C.
	RF_IN	11	AI	GNSS antenna interface	-	50 Ω characteristic impedance.
	ANT_DET2	16	AI	External active antenna detection 2	$V_I$min = 0.3 V $V_I$nom = 3.3 V $V_I$max = 4.5 V	If unused, leave the pins N/C.
	ANT_DET1	17	AI	External active antenna detection 1	$V_I$min = 0.3 V $V_I$nom = 3.3 V $V_I$max = 4.5 V	
	ANT_ON	14	DO	Power control for external active antenna with antenna detection or LNA	V_{OL}max = 0.4 V V_{OH}min = VCC - 0.4 V	If unused, leave the pin N/C.
System	BOOT	6	DI	Controls module startup mode	V_{IL}min = -0.3 V V_{IL}max = 0.8 V V_{IH}min = 2.0 V V_{IH}max = VCC + 0.3 V	Pulled down internally by default. If the pin is pulled up for about 50 ms during startup, the module enters the Boot download mode.
	WAKEUP	1	DI	Wakes up the module from the Standby mode	V_{IH}min = 2.1 V V_{IH}max = VCC	Keep this pin at a low voltage level in the Continuous mode. It is pulled down internally with a 47 kΩ resistor. Drive the pin to a high

Function	Name	No.	I/O	Description	DC Characteristics	Remarks
						voltage level for at least 10 ms to exit the Standby mode. If unused, leave the pin N/C.
	RESET_N	8	DI	Resets the module	V_{IL}min = -0.3 V V_{IL}max = 0.35 V V_{IH}min = 0.65 V V_{IH}max = 1.3 V	Active low. Do not reserve any pull-up circuit for this pin.
GND	GND	10, 12, 13, 24	-	Ground	-	Ensure a good GND connection to all GND pins of the module, preferably with a large ground plane.
RESERVED	RESERVED	2, 4, 5, 7, 15, 18, 19	-	Reserved	-	Pin 2 is RESERVED for L26-DR (AA, ADRC, UDR). Pins 4 and 15 are RESERVED for L26-DR (AA, UDR). These pins must be left N/C and cannot be connected to power or GND.

NOTE

1. Leave RESERVED and unused pins N/C.
2. Operation beyond the operating voltage range indicated by DC characteristics is not recommended and extended exposure beyond the operating voltage range may affect device reliability.

3 Power Management

The module features a power optimized architecture with built-in autonomous energy saving capabilities to minimize power consumption at any given time. The receiver can be used in three operating modes: Standby and Backup modes for optimum power consumption, and Continuous mode for optimum performance.

3.1. Power Unit

VCC is the supply voltage pin of the module. It supplies the PMU, which in turn powers the entire system. The load current of the VCC pin varies according to VCC voltage level, processor load, and satellite acquisition. It is important to supply sufficient current and make sure the power supply is clean and stable.

The V_BCKP pin supplies the backup domain, which includes RTC and SRAM. To achieve quick startup and improve TTFF, the backup domain power supply should be valid at all times. If the VCC is invalid, the V_BCKP supplies the SRAM that contains all the necessary GNSS data and some of the user configuration variables.

VDD_RF is an output pin equal in voltage to the VCC input. In the Continuous mode, VDD_RF supplies the external active antenna or LNA. Only if VCC is cut off, VDD_RF is turned off.

The module's internal power supply is shown below:

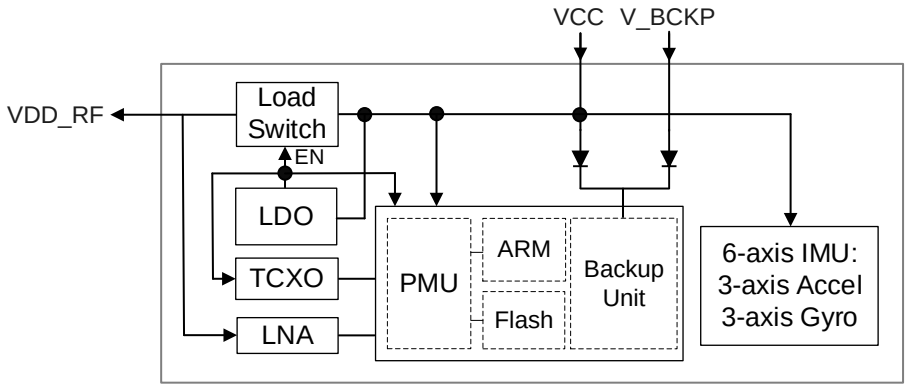


Figure 3: Internal Power Supply

NOTE

L26-DR (AA) does not support the 6-axis IMU.

3.2. Power Supply

3.2.1. VCC

VCC is the supply voltage pin that supplies the BB, RF and 6-axis IMU (not supported by L26-DR (AA)).

Module power consumption may vary by several orders of magnitude, especially when power saving modes are enabled. Therefore, it is important that the power supply is able to sustain peak power for a short time, ensuring that the load current does not exceed the rated value. When the module starts up or switches from the Backup mode to the Continuous mode, VCC must charge the internal capacitors in the core domain. In some cases, this can lead to a significant current drain.

For low-power applications using power saving modes, it is important that the LDO at the power supply or module input is able to provide sufficient current when the module is switched from Backup mode to Continuous mode. An LDO with a high PSRR should be chosen for optimum performance. In addition, a TVS, and a combination of a 10 µF, a 100 nF and a 33 pF decoupling capacitor should be added near the VCC pin. The lowest value capacitor should be the closest to the VCC pin.

A fast-discharging LDO voltage regulator is recommended to ensure a quick voltage drop when the VCC power is removed.

It is not recommended to use a switching DC-DC converter.

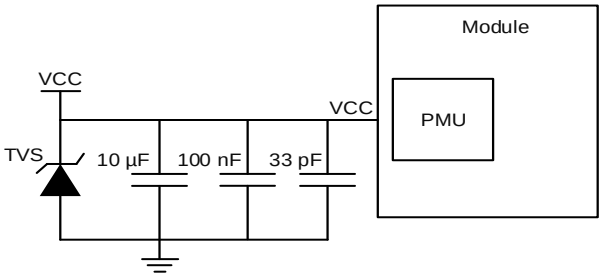


Figure 4: VCC Input Reference Circuit

NOTE

Ensure the module VCC is controlled by MCU to save power, or restart the module when it enters an abnormal state.

3.2.2. V_BCKP

The V_BCKP pin supplies the backup domain. Use of valid time and GNSS orbit data at startup allows GNSS hot (warm) start. V_BCKP must be connected to the power supply for startup, and it should be always powered if hot (warm) start is needed.

If there is a constant power supply in your system, it can be used to provide a suitable voltage to power V_BCKP.

It is recommended to place a TVS and a combination of a 4.7 μF, a 100 nF, and a 33 pF decoupling capacitor near the V_BCKP pin. The figure below illustrates the reference design for powering the backup domain.

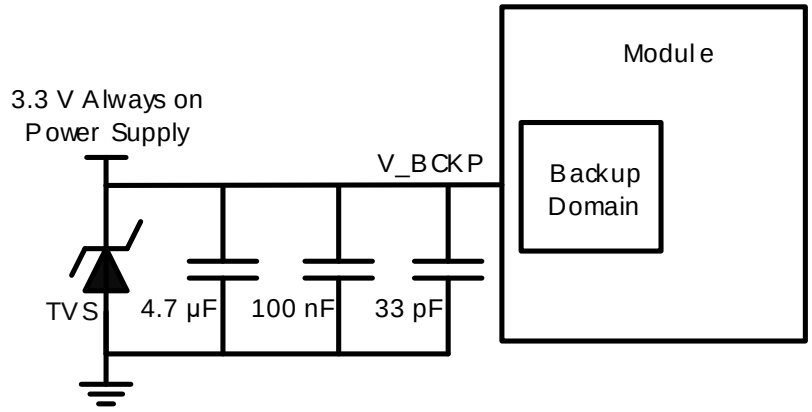


Figure 5: Backup Domain Input Reference Circuit

For L26-DR (UDR), V_BCKP can also be powered by a 3.7 V lithium battery. It is recommended to use MCU to control the enable pin of LDO via MCU, as shown below.

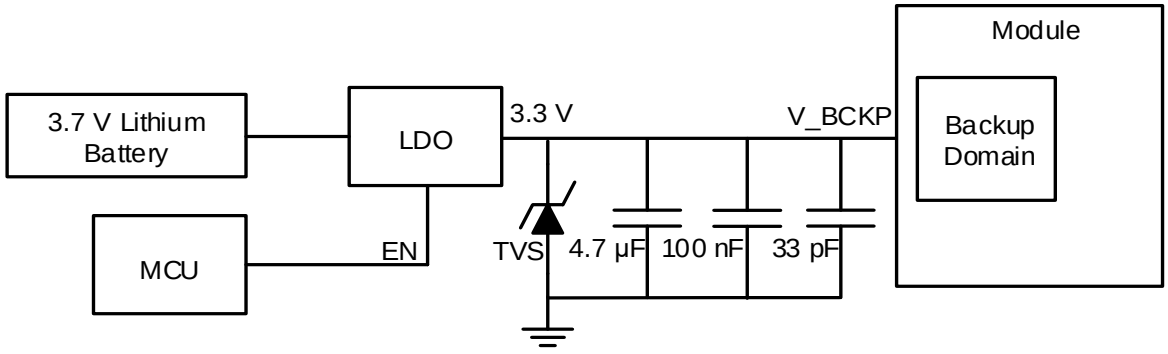


Figure 6: Reference Power Supply Circuit with 3.7 V Lithium Battery for L26-DR (UDR)

NOTE

1. If V_BCKP is below the minimum value of the recommended operating voltage, the module cannot work normally.
2. It is recommended to control the module V_BCKP via MCU to restart the module when it enters an abnormal state.

3.3. Power Modes

3.3.1. Feature Comparison

The module features supported in different modes are listed in the table below.

Table 7: Feature Comparison in Different Power Modes

Feature	Continuous	Standby	Backup
NMEA from UART	●	-	-
1PPS	●	-	-
RF	●	-	-
Acquisition & Tracking	●	-	-
Power Consumption	High	Low	Low
Position Accuracy	High	-	-

3.3.2. Continuous Mode

If VCC and V_BCKP are powered on, the module automatically enters the Continuous mode that comprises acquisition mode and tracking mode. In acquisition mode, the module starts to search satellites, and determine visible satellites, coarse frequency, as well as the code phase of satellite signals. Once the acquisition is completed, the module automatically switches to tracking mode. In tracking mode, the module tracks satellites and demodulates the navigation data from specific satellites.

3.3.3. Standby Mode

The Standby mode is a power saving mode, in which the internal core, I/O power domain, and RF are powered off. UART is not accessible, and the module stops acquiring and tracking satellites. However, the 6-axis IMU (not supported by L26-DR (AA)) and backup domain are still active. When the module exits

the Standby mode, it will use internal ancillary information, such as GPS time, ephemeris, and last position to ensure the fastest possible TTFF during hot or warm start.

There is one way to enter and two ways to exit the Standby mode.

- Enter the Standby mode:
  Send the **PSTMFORCESTANDBY**.

- Exit the Standby mode:
  - Pull up WAKEUP pin for at least 10 ms; **OR**
  - Wait for the Standby time duration set by **PSTMFORCESTANDBY** to end.

For details of the related software command, see *document [1] protocol specification*.

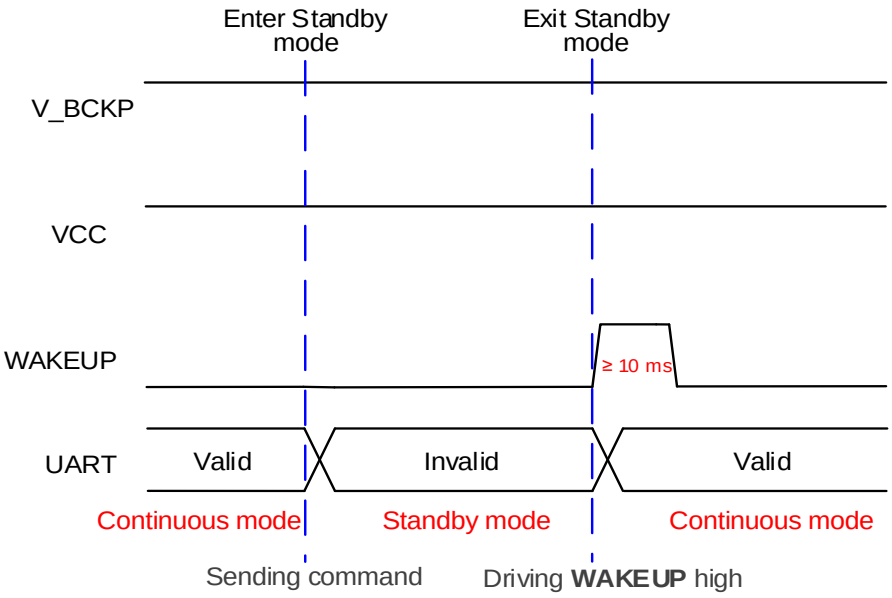


Figure 7: Sequence for Entering/Exiting Standby Mode

NOTE

Before executing **PSTMFORCESTANDBY** to enter the Standby mode, ensure that the WAKEUP pin is not pulled up, otherwise the module will enter an indeterminate state.

3.3.4. Backup Mode

For power-sensitive applications, the module supports the Backup mode to reduce power consumption. Only the backup domain is active in the Backup mode and it keeps track of time.

- Enter the Backup mode:
  1. Send **PSTMFORCESTANDBY** to shut down the internal main power supply in sequence.
  2. After 350 ms, cut off the power supply to the VCC pin and keep the V_BCKP powered.

- Exit the Backup mode:
  1. Restore VCC.
  2. Pull up the WAKEUP pin for at least 10 ms.

For details of the related software command, see *document [1] protocol specification*.

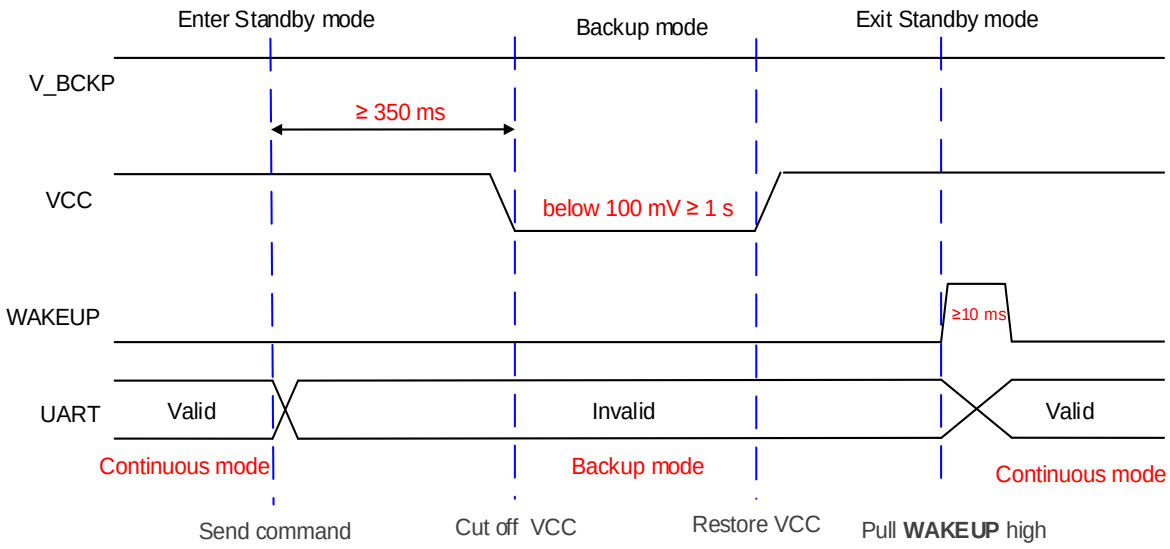


Figure 8: Enter/Exit Backup Mode Sequence

NOTE

1. After restoring VCC, the WAKEUP pin must be pulled up for at least 10 ms for the module to exit the Standby mode. Otherwise, the UART will be inaccessible.
2. Ensure a stable V_BCKP voltage without rush or drop when the VCC is switched on or off.
3. The **PSTMFORCESTANDBY** must be sent to shut down the internal main power supply and the V_BCKP must be kept powered to ensure a hot (warm) start at the module's next startup.

3.4. Power-up Sequence

Once the VCC and V_BCKP are powered up, the module starts up automatically and the voltage should rise rapidly in less than 50 ms.

To ensure the correct power-up sequence, the backup unit should start up no later than the PMU. Hence, the V_BCKP must be powered simultaneously with the VCC or before it.

Ensure that the VCC and V_BCKP have no rush or drop during the rising time, and then keep them stable. The recommended ripple is < 50 mV.

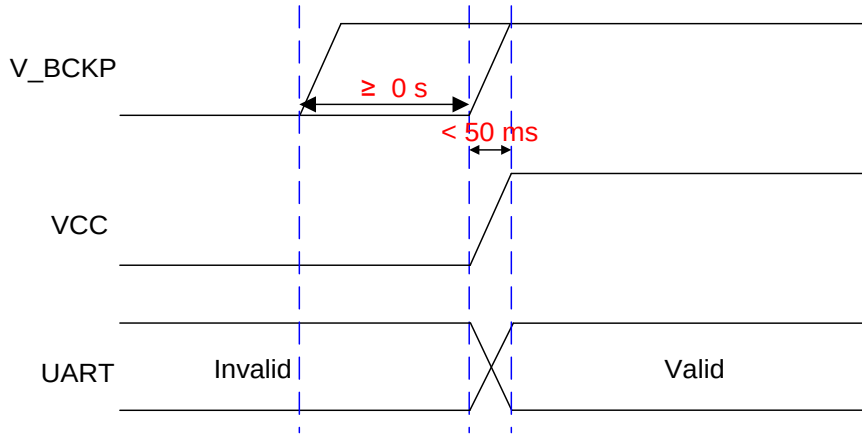


Figure 9: Power-up Sequence

3.5. Power-down Sequence

Once the VCC and V_BCKP are shut down, the module turns off automatically and voltage should drop quickly in less than 50 ms. It is recommended to use a voltage regulator that supports fast discharging.

To avoid abnormal voltage conditions, if VCC and V_BCKP fall below the minimum specified value, the system must initiate a power-on restart by lowering VCC and V_BCKP to less than 100 mV for at least 1 s.

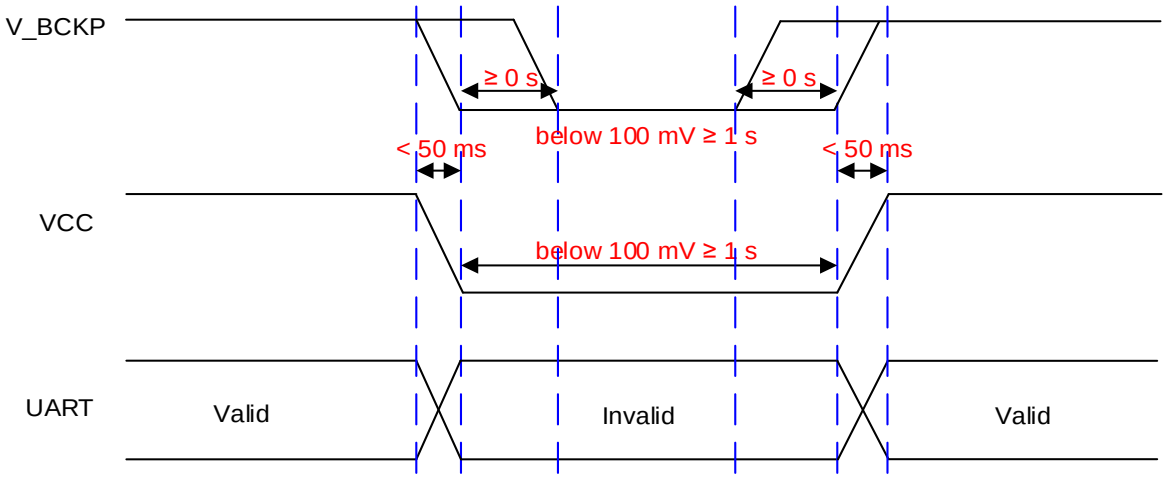


Figure 10: Power-down and Power-on Restart Sequence

4 Application Interfaces

4.1. I/O Pins

4.1.1. Communication Interface

The following interface can be used for data reception and transmission.

4.1.1.1. UART Interface

The module has one UART interface with the following features:

- Supports standard NMEA message, PSTM message, speed information (not supported by L26-DR (AA, UDR)) and firmware upgrade.
- Supports the following baud rates: 115200, 230400, 460800, and 921600 bps.
- Hardware flow control and synchronous operation are not supported.

For more information, see *document [1] protocol specification*.

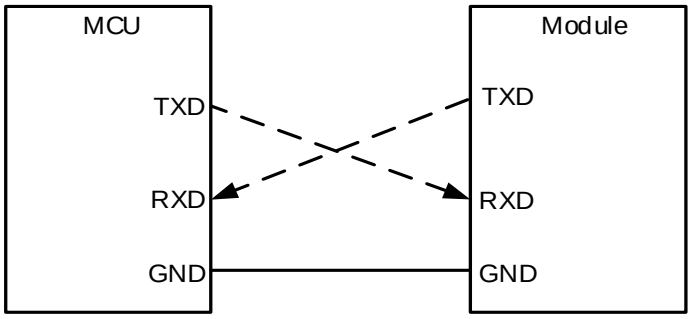


Figure 11: UART Interface Reference Design

A reference design is shown in the figure above. For more information, see *document [6] reference design*.

NOTE

1. UART interface default settings may vary depending on software versions. See specific software versions for details.
2. If the I/O voltage of the MCU does not match the module, a level-shifting circuit must be selected.

4.1.2. FWD

The L26-DR (ADR, ADRC) support the FWD pin to input the status signals indicating the forward/backward movement of a vehicle. When the pin is at a low voltage level, the vehicle is moving forward, and when it is at a high level, the vehicle is moving backward.

NOTE

When using the Wheel Tick Mode to obtain speed information, ensure that the FWD pin is connected on L26-DR (ADR, ADRC).

4.1.3. WHEELTICK

The L26-DR (ADR, ADRC) support the WHEELTICK pin to input wheel tick pulse signals from a vehicle, which are obtained from the wheel revolution sensors or vehicle transmission. For more information about the reference design of this interface, see *document [6] reference design*.

NOTE

When using the Wheel Tick Mode to obtain speed information, ensure that the WHEELTICK pin is connected on L26-DR (ADR, ADRC).

4.1.4. WI

The L26-DR (ADR) supports the WI pin, which provides an interrupt output to wake up the host when the 6-axis IMU value exceeds the threshold value. However, the module cannot determine the cause of vehicle tilting. Therefore, the code running on the MCU must assess other parameters to determine whether the vehicle is being towed or is running normally on a hilly road.

NOTE

To ensure interrupt signal output, ensure that the module's VCC pin is powered normally.

4.1.5. 1PPS

The 1PPS output pin generates periodic time pulse signals synchronized with a GNSS time grid at regular intervals. This feature allows the pin to maintain high accuracy, provided that the modules have visible satellites in an open sky environment and a powered VCC. See *Table 3: Product Performance* for details about pulse accuracy.

4.2. System Pins

4.2.1. WAKEUP

WAKEUP pin is pulled down internally with a 47 kΩ resistor. It is used for waking up the module from the Standby mode by being driven to a high voltage level for at least 10 ms. Keep this pin at a low voltage level in the Continuous mode.

4.2.2. RESET_N

RESET_N is an input pin. The module can be reset by driving RESET_N pin low for at least 100 ms and then releasing it.

By default, RESET_N pin is internally pulled up to 1.0 V with a 10 kΩ resistor, and thus no external pull-up circuit is allowed for this pin.

An OC driver circuit as shown below is recommended to control the RESET_N pin.

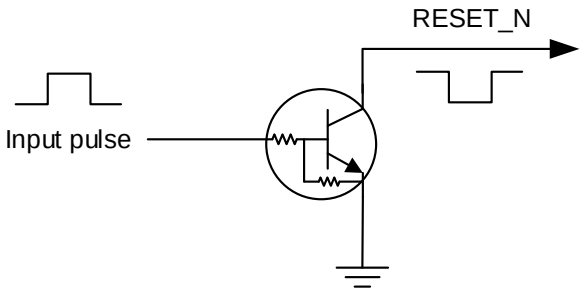


Figure 12: Reference OC Circuit for Module Reset

The following figure shows the reset sequence of the module.

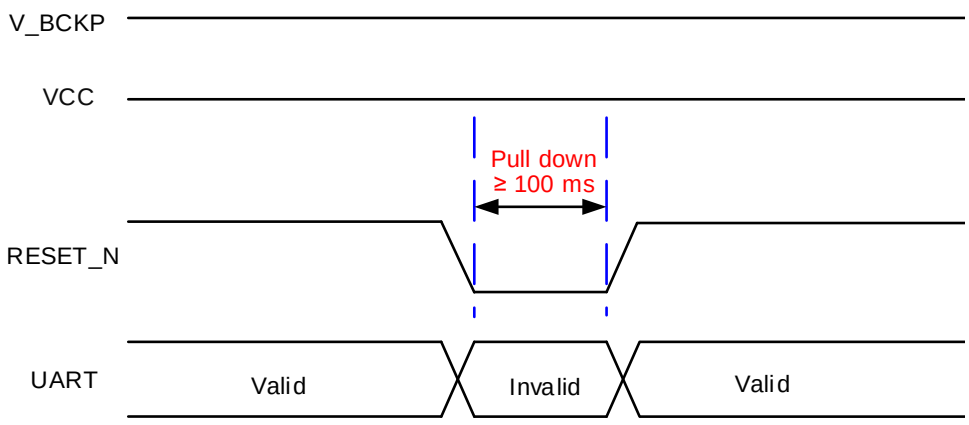


Figure 13: Reset Sequence

NOTE

RESET_N pin must be connected so that it can be used to reset the module if it enters an abnormal state.

4.2.3. BOOT

The BOOT pin can be used to set the module to the Boot download mode. It is pulled down internally by default. For more information about the reference design, see *document [6] reference design*.

The BOOT pin voltage level is checked automatically to identify the module's operating mode when the module is powered on.

Table 8: Operating Modes

Voltage Level	Operating Mode	Comment
Low	Normal	The BOOT pin is pulled down internally by default.
High	Boot Download	If the pin is kept at a high level for about 50 ms during startup, the module enters the Boot download mode.

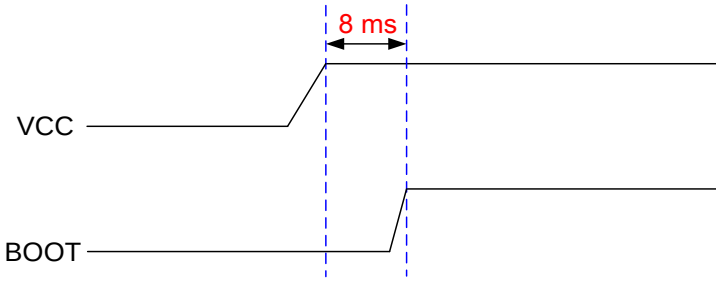


Figure 14: BOOT Pin State (Normal Operating Mode)

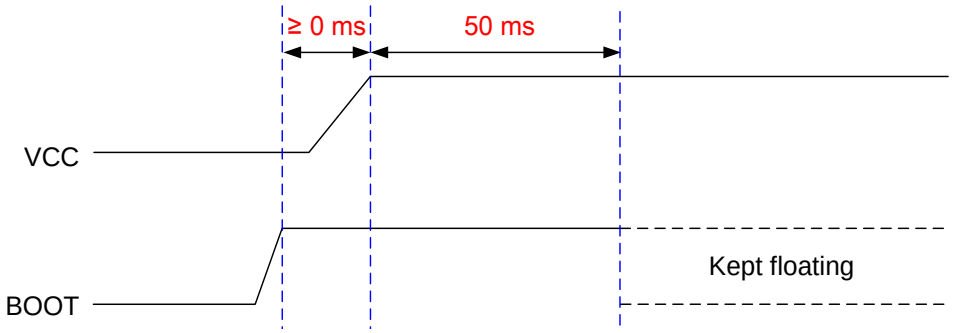


Figure 15: BOOT Pin Control Sequence (Boot Download Mode)

4.3. Avoiding Current Leakage on I/O Pins

This chapter provides important design considerations for the module current leakage in Backup mode and the complete power-off power state of the module, which are defined as follows:

- In Backup mode, the module's VCC power pin is disconnected while the V_BCKP pin is still powered.
- In the complete power-off state, all power pins (V_BCKP and VCC) of the module are powered off.

In the above two power states, when there is an external voltage on the module's I/O pins, the power consumption in Backup mode will increase, and there will be residual voltage on VCC pin, whereas the external voltage can cause parasitic leakage current to flow through the module in the completely powered-off state, leading to energy loss. To prevent current leakage or parasitic leakage current, no external voltage is allowed on the module's I/O pins. Two recommended ways to accomplish this are to:

1. Pull down all I/O pins connected to the module when it enters Backup mode or is completely powered off, while the host is still working.

2. Use components that prevent backflow current from passing through when the power is turned off, specifically designed for power-off applications. The noninverting buffer with output-enable (OE)

control is recommended to provide isolation. When the OE of the enable pin is low, the output end of the noninverting buffer enters a high-resistance state. For UART communication between the module and host, we recommend the following design:

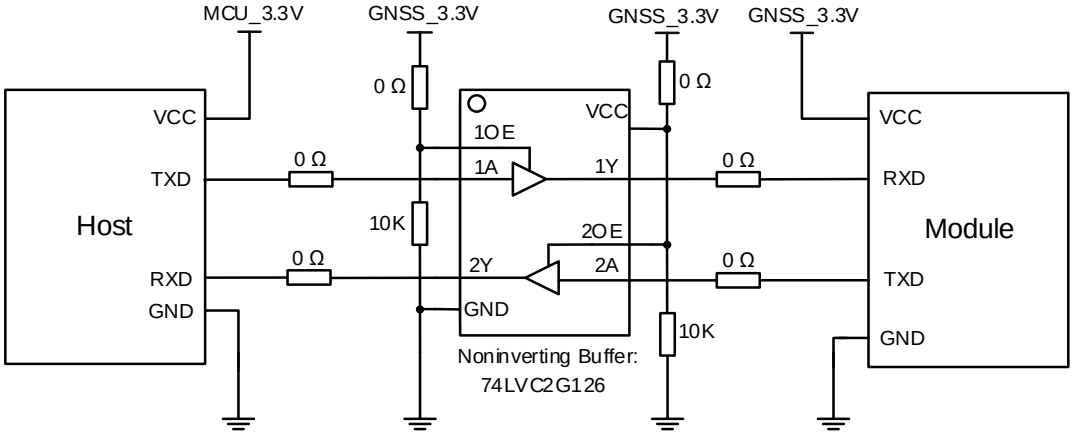


Figure 16: Noninverting Buffer Circuit Between Module and Host

5 Design

This chapter explains the reference design of the RF section and recommended footprint of the module. GNSS receiver could be vulnerable to environmental interference. To learn the details about interference and ensuring interference immunity, see *document [7] GNSS antenna application note*.

5.1. Antenna Specifications

The module can be connected to a dedicated passive or an active single-band GNSS antenna to track the GNSS satellite signals. The recommended antenna specifications are given in the table below.

Table 9: Recommended Antenna Specifications

Antenna Type	Specifications
Passive Antenna	Frequency range: 1559–1606 MHz Polarization: RHCP VSWR: < 2 (Typ.) Passive Antenna Gain: > 3 dBi
Active Antenna	Frequency Range: 1559–1606 MHz Polarization: RHCP VSWR: < 2 (Typ.) Passive Antenna Gain: > 3 dBi Active Antenna Noise Figure: ≤ 2.5 dB Active Antenna Total Gain: < 17 dB [6] Axial Ratio: < 3 dB -3 dB Beam Width: > 90° Out-of-band Rejection: > 30 dB

NOTE

For recommended antenna and design, see *document [7] GNSS antenna application note* or contact Quectel Technical Support (support@quectel.com).

[6] The total antenna gain equals the internal LNA gain minus the total insertion loss of cables and components inside the antenna.

5.2. Antenna Reference Design

To mitigate the impact of out-of-band signals on the GNSS module in a complex electromagnetic environment, a SAW filter circuit must be added to the antenna design. The SAW filter circuit has a stable suppression effect on all out-of-band signals. In the actual layout, the circuit should be placed close to RF_IN pin. The SAW filter circuit should be selected according to the use case.

NOTE

For recommended SAW models, contact Quectel Technical Support (support@Quectel.com).

5.2.1. ANT_DET1 and ANT_DET2

The ANT_DET1 and ANT_DET2 are analog input pins for detecting external active antenna status. Through an antenna detection circuit, the state of the antenna (normal/open/short) can be judged by ANT_DET1 and ANT_DET2. See *Chapter 5.2.2.2 Active Antenna Reference Design with Antenna Detection Function* for details.

5.2.2. Active Antenna Reference Design

If the active antenna is supplied by VDD_RF pin, it is important to consider the operating voltage range of the antenna and the voltage drop on the power supply circuit. The voltage drop is caused by the resistor (R2) and the inductor (L1) in the external power supply circuit. To further mitigate the impact of out-of-band signals on the GNSS module, you must choose the active antenna whose SAW filter is placed in front of the LNA in the internal framework. DO NOT place the LNA in the front. The minimum operating voltage of the selected active antenna must meet the circuit design characteristics.

5.2.2.1. Active Antenna Reference Design Without Antenna Detection Function

A typical reference design of an active antenna without antenna detection function is presented below.

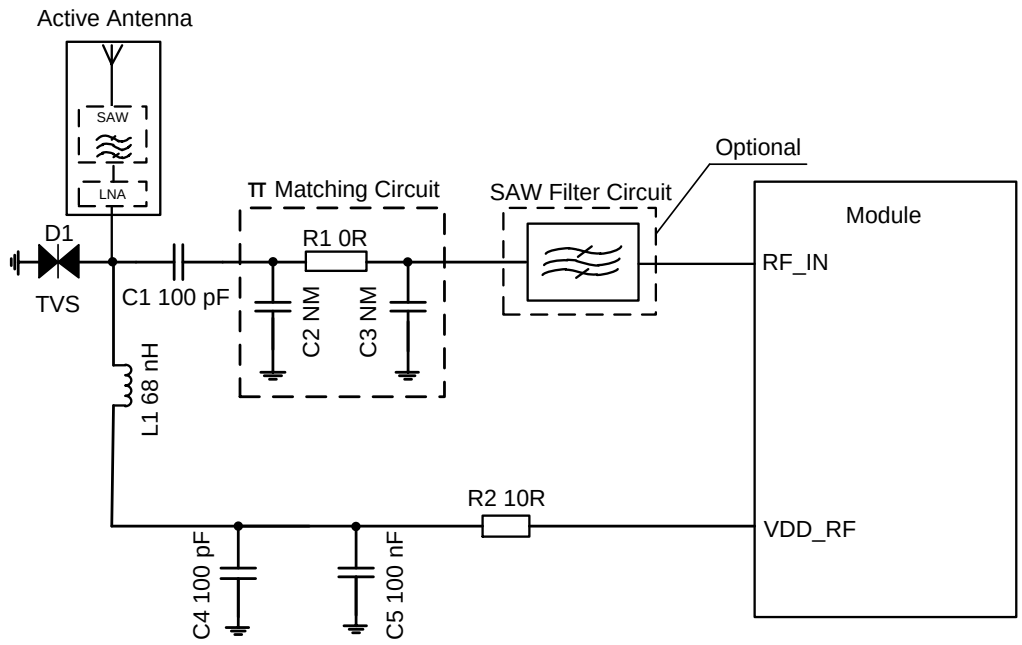


Figure 17: Active Antenna Reference Design Without Antenna Detection Function

C1 is a DC-blocking capacitor used for blocking the DC current from VDD_RF. The C2, R1, and C3 components are reserved for matching antenna impedance. By default, C1 is 100 pF; R1 is 0 Ω, while C2 and C3 are not mounted. They should be placed near the antenna in the actual layout. D1 is an electrostatic discharge (ESD) protection device to protect RF signal input from the potential damage caused by ESD. The junction capacitance of D1 cannot be more than 0.6 pF and a transient voltage suppressor is recommended.

L1 inductor is used for preventing the RF signal from leaking into the VDD_RF and preventing noise propagation from the VDD_RF to the antenna. L1 inductor routes the bias voltage to the active antenna without losses. Place L1, C4 and C5 close to the antenna interface and route the proximal end of L1 pad on the RF trace. The recommended value of L1 should be at least 68 nH. R2 resistor is used to protect the module in case the active antenna is short-circuited to the ground plane. RF trace impedance should be controlled to 50 Ω and trace length should be kept as short as possible. For more information about RF layout, see *document [8] RF layout application note*.

5.2.2.2. Active Antenna Reference Design with Antenna Detection Function

A typical reference design of an active antenna with antenna detection function is presented below.

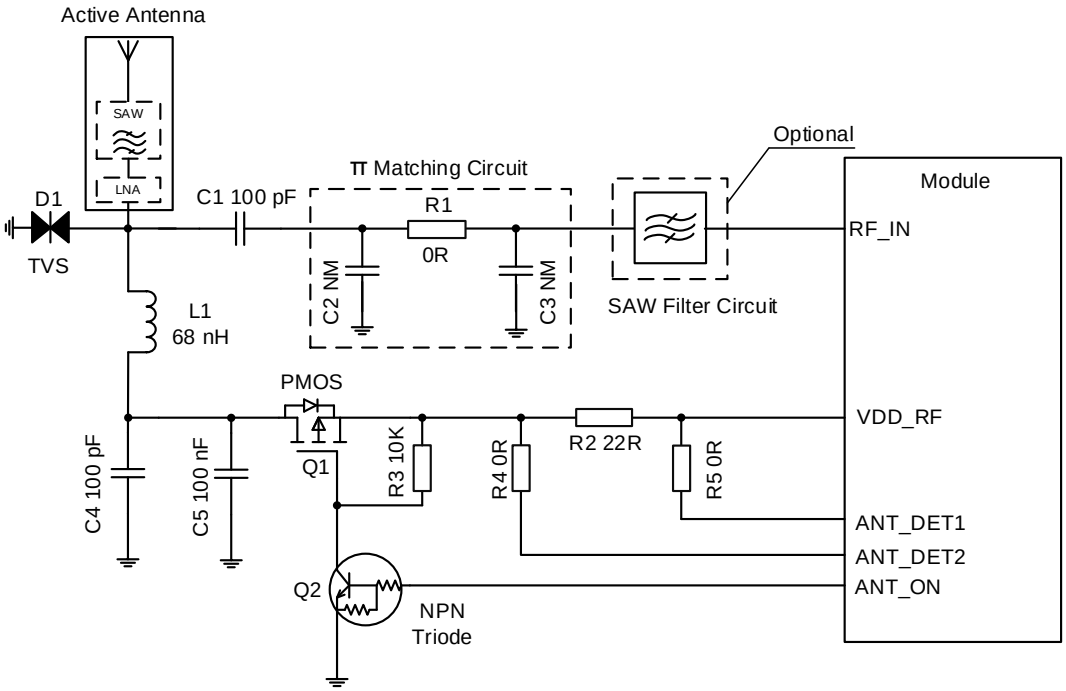


Figure 18: Active Antenna Reference Design with Antenna Detection Function

The module reads the state of the antenna (normal/open/short) through the antenna detection circuit. The circuit uses two analog inputs, ANT_DET1 and ANT_DET2 pins, to compare the voltages at both ends of the R2 resistor (22 Ω recommended).

The ANT_ON pin controls the power supply for the active antenna with antenna detection function. When ANT_ON is at a high level, both transistors Q1 and Q2 will be switched on and the external antenna will be powered by VDD_RF. When ANT_ON is at a low level, both Q1 and Q2 will be switched off, thus disabling the external antenna. VDD_RF will be powered off automatically only in the Backup mode.

Ensure that the antenna power consumption falls within the 7–30 mA range, otherwise the active antenna may not work. The status of the antenna detection circuit will be reported in an NMEA message at startup and on each change. For more information about the NMEA message, see *document [1] protocol specification*.

5.2.3. Passive Antenna Reference Design

A typical reference design of a passive antenna is illustrated in the following figure.

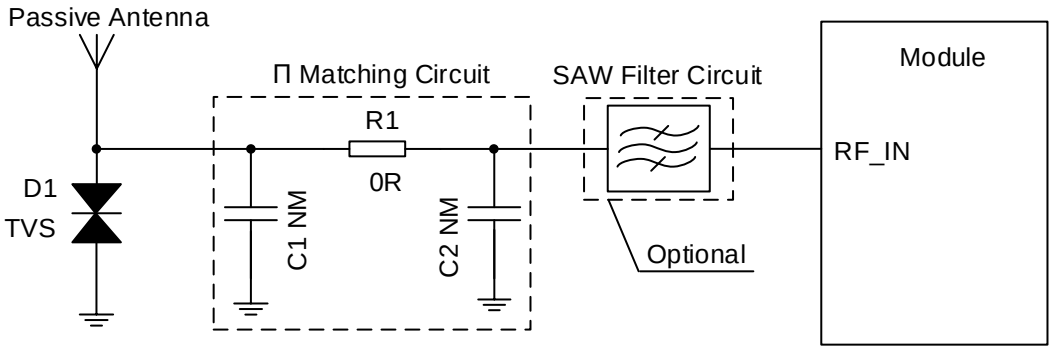


Figure 19: Passive Antenna Reference Design

C1, R1, and C2 are reserved for matching antenna impedance. By default, R1 is 0 Ω, and C1 and C2 are not mounted. They should be placed near the antenna in the actual layout. D1 is an electrostatic discharge (ESD) protection device to protect RF components inside the module from the damage caused by ESD through the antenna interface. The junction capacitance of D1 cannot be more than 0.6 pF and a transient voltage suppressor is recommended. RF trace impedance should be controlled to 50 Ω and the trace length should be kept as short as possible.

5.3. Recommended Footprint

The figure below illustrates a module footprint. These are recommendations, not specifications.

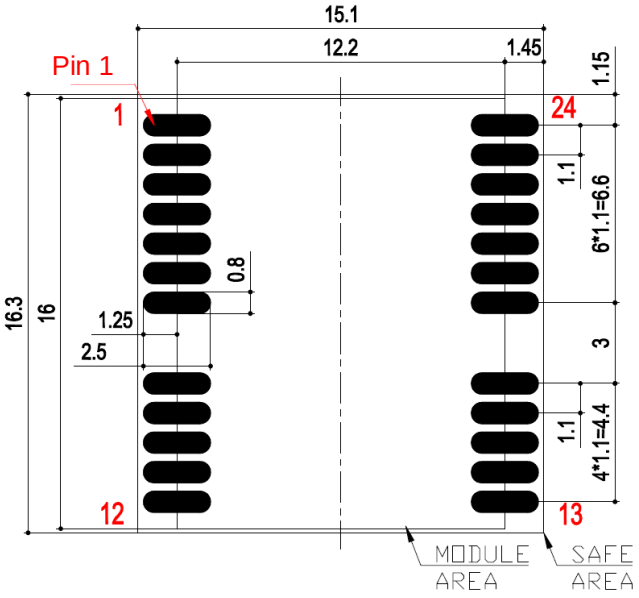


Figure 20: Recommended Footprint

NOTE

Maintain at least 3 mm keepout between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6 Electrical Specification

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital pins of the module are listed in the table below.

Table 10: Absolute Maximum Ratings

Parameter	Description	Min.	Max.	Unit
VCC	Main Power Supply Voltage	-0.3	3.6	V
V_BCKP	Backup Supply Voltage	-0.3	3.6	V
V_{IN}_IO	Input Voltage at I/O Pins	-0.2	VCC + 0.3	V
P_{RF_IN}	Input Power at RF_IN	-	0	dBm
T_storage	Storage Temperature	-40	95	°C

NOTE

Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. The product is not protected against over-voltage or reversed voltage. Therefore, it is necessary to use appropriate protection diodes to keep voltage spikes within the parameters given in the table above.

6.2. Power Consumption Requirement

The following table lists the power consumption values of the total system that may be applied. Actual power requirements may vary depending on processor load, external circuits, firmware version, the number of tracked satellites, signal strength, startup type and test duration.

Table 11: Power Consumption for L26-DR (AA, UDR)

Parameter	Description	Condition	L26-DR (AA)		L26-DR (UDR)	
			$I_{Typ.}$ [7]	I_{PEAK} [7]	$I_{Typ.}$ [7]	I_{PEAK} [7]
I_{VCC} [8]	Current at VCC	Acquisition	81 mA	118 mA	84 mA	120 mA
		Tracking	81 mA	118 mA	81 mA	120 mA
		Standby Mode	1.7 mA	2.4 mA	1.7 mA	2.4 mA
I_{V_BCKP} [9]	Current at V_BCKP	Continuous Mode	125 μA	158 μA	102 μA	135 μA
		Standby Mode	8 μA	43 μA	8 μA	43 μA
		Backup Mode	8 μA	43 μA	8 μA	43 μA

Table 12: Power Consumption for L26-DR (ADR, ADRC)

Parameter	Description	Condition	L26-DR (ADR)		L26-DR (ADRC)	
			$I_{Typ.}$ [7]	I_{PEAK} [7]	$I_{Typ.}$ [7]	I_{PEAK} [7]
I_{VCC} [8]	Current at VCC	Acquisition	81 mA	117 mA	81 mA	117 mA
		Tracking	80 mA	117 mA	80 mA	117 mA
		Standby Mode	1.7 mA	2.4 mA	1.7 mA	2.4 mA
I_{V_BCKP} [9]	Current at V_BCKP	Continuous Mode	122 μA	156 μA	122 μA	157 μA
		Standby Mode	8 μA	43 μA	8 μA	43 μA
		Backup Mode	8 μA	43 μA	8 μA	43 μA

NOTE

The above power consumption values are measured within the respective modes, excluding transient pulse currents that occur during power-up and mode transition.

[7] Tested at room temperature, with typical operating voltage, and satellites signal of -130 dBm configured by the instrument.
[8] Used to determine maximum current capability of power supply.
[9] Used to determine required battery current capability.

6.3. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wearing anti-static gloves during the development, production, assembly, and testing of the module; adding ESD protective components to the ESD sensitive interfaces and points in the product design.

Measures to ensure protection against ESD damage when handling the module:

- When mounting the module onto a motherboard, make sure to connect the GND first, and then the RF_IN pin.
- When handling the RF_IN pin, do not come into contact with any charged capacitors or materials that may easily generate or store charges (such as patch antenna, coaxial cable, and soldering iron).
- When soldering the RF_IN pin, make sure to use an ESD safe soldering iron (tip).

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are in millimeters (mm). The dimensional tolerances are ±0.20 mm, unless otherwise specified.

7.1. Top, Side, and Bottom View Dimensions

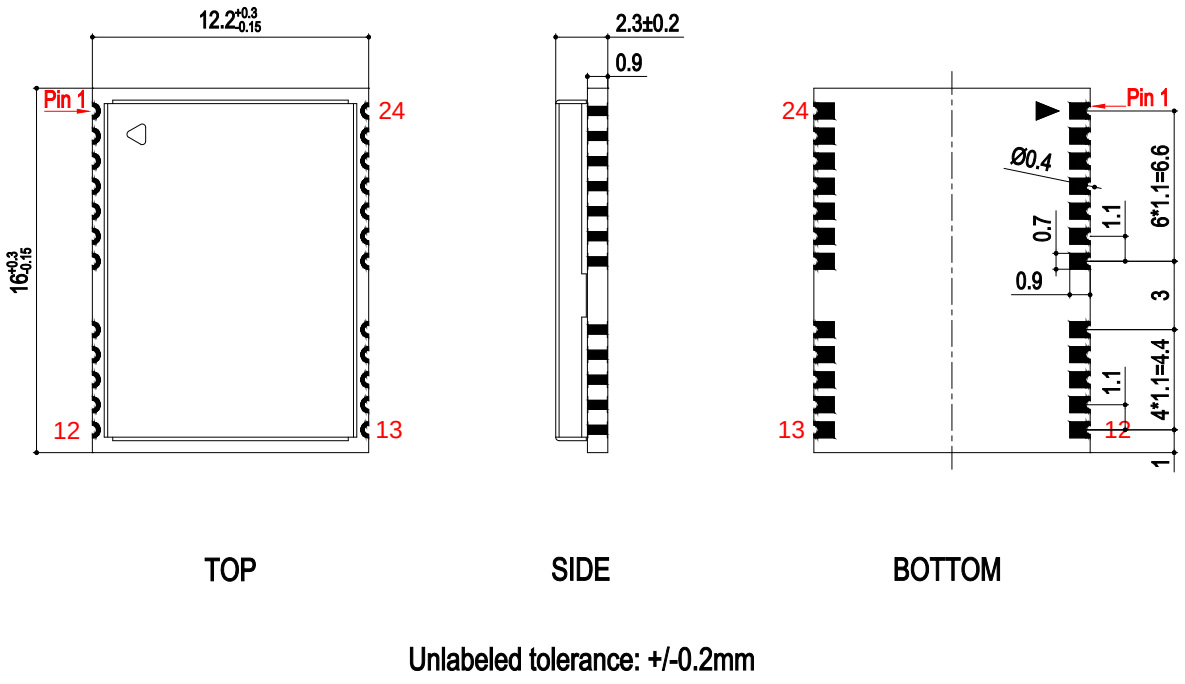


Figure 21: Top, Side, and Bottom View Dimensions

NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2. Top and Bottom Views

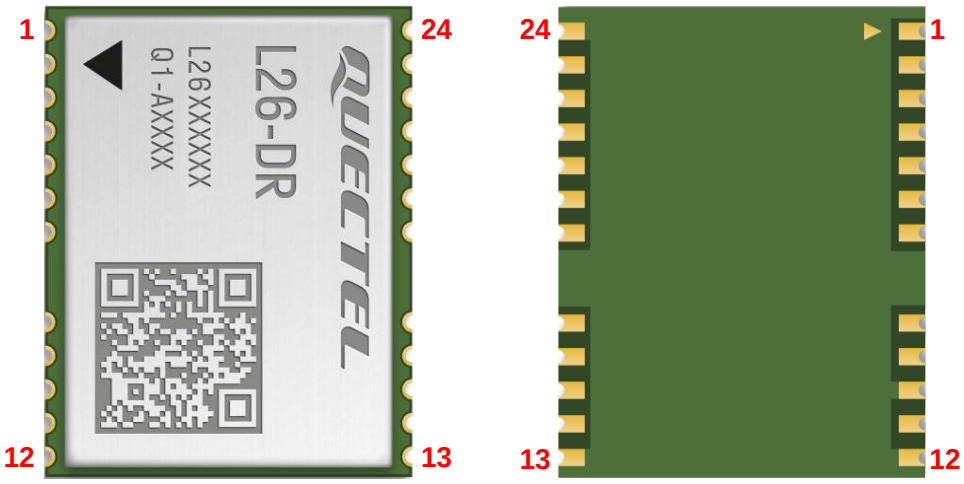


Figure 22: Top and Bottom Views

NOTE

The images above are for illustrative purposes only and may differ from the actual module. For authentic appearance and label, see the module received from Quectel.

7.3. Recommended Mounting

L26-DR (ADR) allows for flexible installation without constraints on angle and direction. The module will automatically recognize the mounting angle deviation and compensate for the deviation by algorithmic calculations.

The installation of the L26-DR (ADRC) module requires that the projection of at least one axis on the plane of the vehicle must be parallel to the direction of vehicle's front.

The installation of L26-DR (UDR) is relatively more demanding. One of the x, y, and z axes, shown in the following figure, should be perpendicular to the horizontal plane, and the deviation should be less than 15°. In this case, there is no limit to the placement direction on the plane formed by the other two axes. In other words, if axis z is perpendicular to the horizontal plane, there is no limit to the mounting direction of the module on the module plane (i.e., the plane formed by x and y axes).

For more information, see *documents [3]* and *[4] DR application notes*.

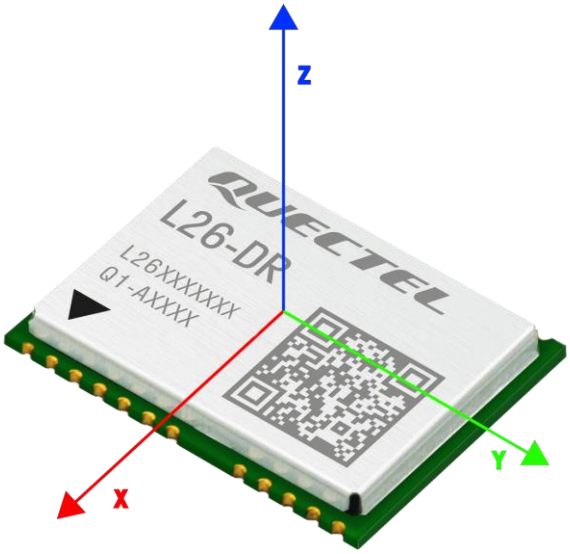


Figure 23: Axes of Module

The module must be tightly mounted on the vehicle in a way that can be considered fixed to the reference frame.

8 Product Handling

8.1. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.1.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

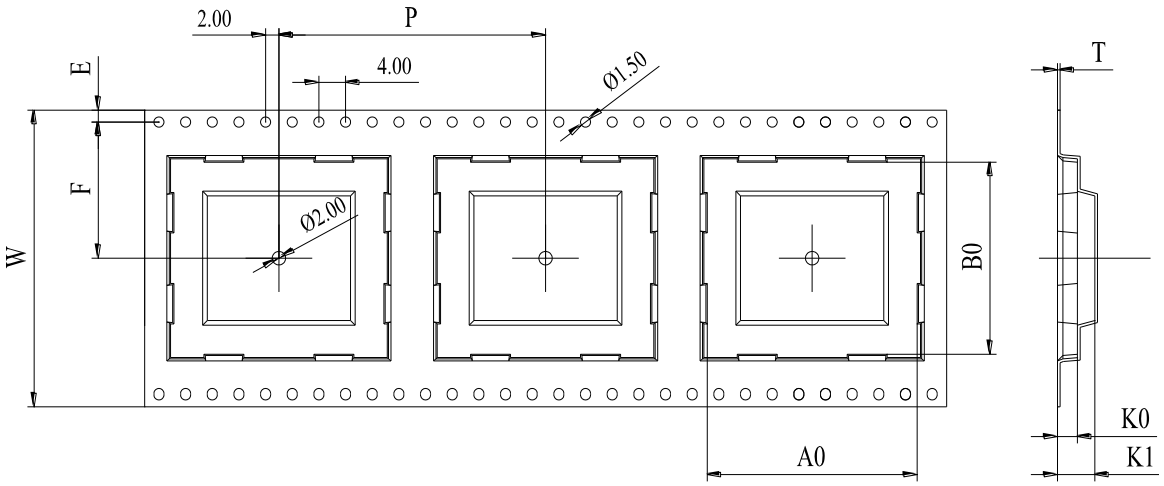


Figure 24: Carrier Tape Dimension Drawing (Unit: mm)

Table 13: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
32	24	0.4	12.7	16.4	2.9	7.4	14.2	1.75

8.1.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

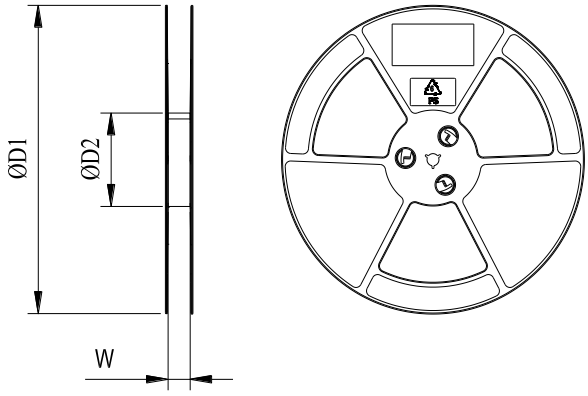


Figure 25: Plastic Reel Dimension Drawing

Table 14: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	32.5

8.1.3. Mounting Direction

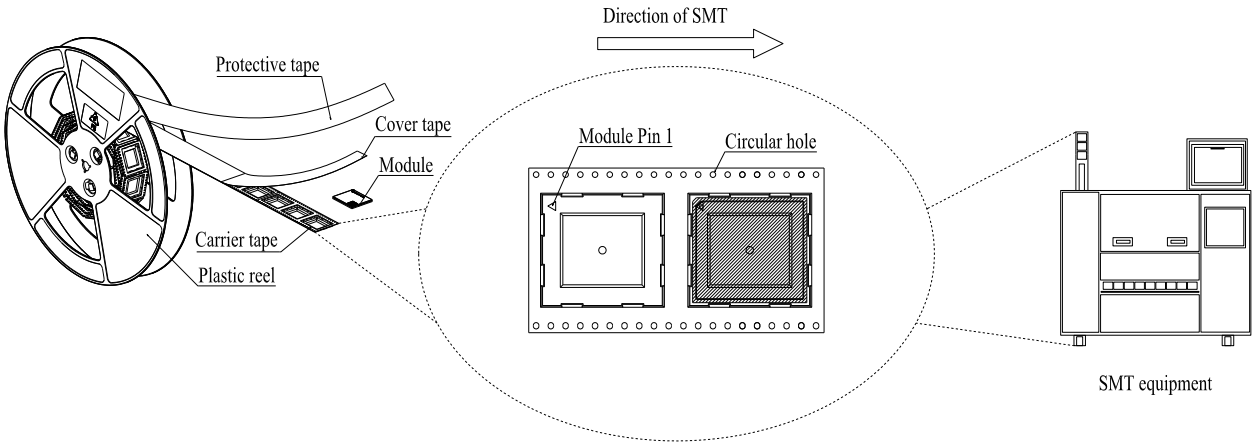
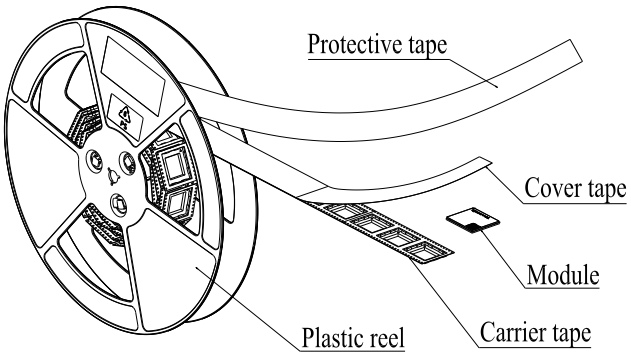


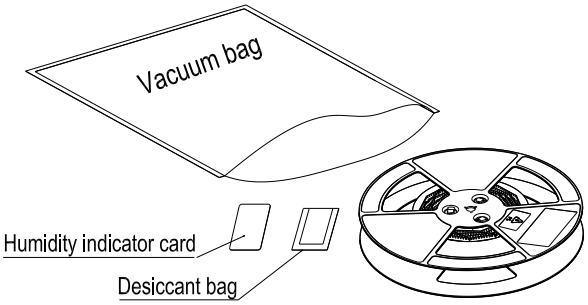
Figure 26: Mounting Direction

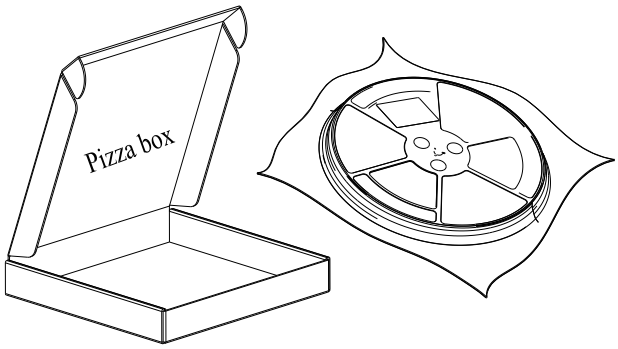
8.1.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 250 modules.

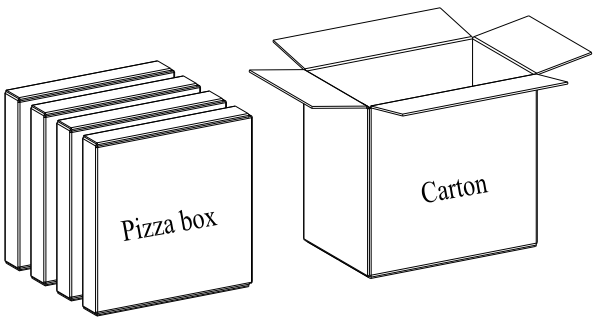
Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.



Pizza box size (mm): 365 × 345 × 56
Carton size (mm): 380 × 250 × 365

Figure 27: Packaging Process

8.2. Storage

The module is provided in vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are listed below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [10] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If pre-baking is needed, it should follow the requirements below:

   - The module should be baked for 24 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as a dry cabinet.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the module.

[10] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

8.3. Manufacturing and Soldering

Push the squeegee to apply solder paste on the stencil surface, thus making the paste fill the stencil openings and then penetrate the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. For more information about the stencil thickness of the module, see *document [9] module stencil design requirements*.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid module damage caused by repeated heating, it is recommended to mount the module only after reflow soldering the other side of the PCB. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown in the figure and table below.

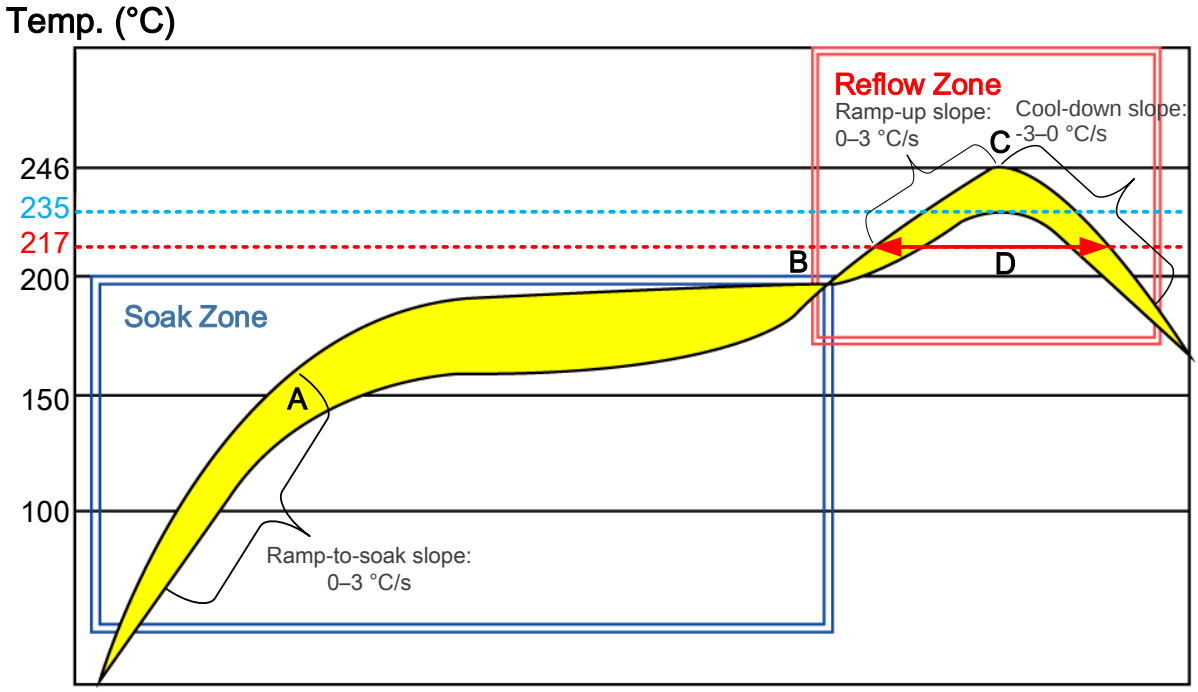


Figure 28: Recommended Reflow Soldering Thermal Profile

Table 15: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s

Factor	Recommended Value
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217 °C)	40–70 s
Max. Temperature	235–246 °C
Cool-down Slope	-3–0 °C/s
Reflow Cycle	
Max. Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may require direct contact with the module, **NEVER** wipe the module shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, and trichloroethylene. Otherwise, the shielding can may become rusty.
3. The module shielding can is made of cupronickel base material. The Neutral Salt Spray Test has shown that after 12 hours the laser-engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, **DO NOT** use any coating material that may react with the PCB or shielding cover. Prevent the coating material from entering the module shield.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
8. Due to SMT process complexity, contact Quectel Technical Support in advance regarding any ambiguous situation, or any process (e.g., selective soldering, ultrasonic soldering) that is not addressed in *document [10] module SMT application note*.

9 Labelling Information

The label of Quectel GNSS modules contains important product information. The location of the product type number is shown in the figure below.

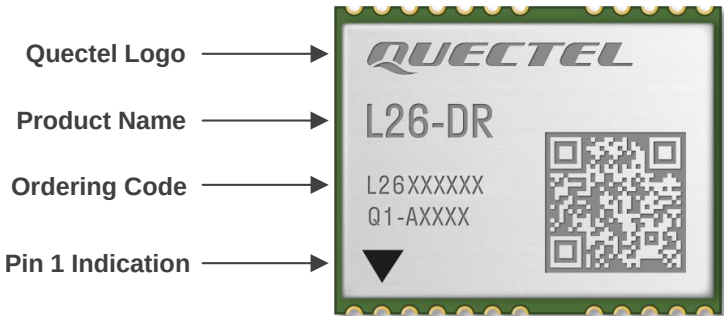


Figure 29: Labelling Information

The image above is for illustrative purposes only and may differ from the actual module. For authentic appearance and label, see the module received from Quectel.

10 Appendix References

Table 16: Related Documents

Document Name
[1] Quectel_L26-DR&L26-P&L26-T&LC98S_Series_GNSS_Protocol_Specification
[2] Quectel_L89&L26-DR&L26-P&L26-T_AGNSS_Application_Note
[3] Quectel_L26-DR(ADR)_DR_Application_Note
[4] Quectel_L26-DR(UDR&ADRC)_DR_Application_Note
[5] Quectel_L26-DR&L26-P&L26-T&L89&LC98S_Firmware_Upgrade_Guide
[6] Quectel_L26-DR_Series_Reference_Design
[7] Quectel_GNSS_Antenna_Application_Note
[8] Quectel_RF_Layout_Application_Note
[9] Quectel_Module_Stencil_Design_Requirements
[10] Quectel_Module_SMT_Application_Note

Table 17: Terms and Abbreviations

Abbreviation	Description
1PPS	1 Pulse Per Second
AGNSS	Assisted GNSS (Global Navigation Satellite System)
ADR	Automotive Dead Reckoning
BB	Baseband
BDS	BeiDou Navigation Satellite System
bps	bit(s) per second

Abbreviation	Description
CAN	Controller Area Network
CEP	Circular Error Probable
DR	Dead Reckoning
EGNOS	European Geostationary Navigation Overlay Service
ESD	Electrostatic Discharge
GAGAN	GPS Aided Geo Augmented Navigation
Galileo	Galileo Satellite Navigation System (EU)
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
I/O	Input/Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
IMU	Inertial Measurement Unit
I_{PEAK}	Peak Current
NavIC	Indian Regional Navigation Satellite System
LCC	Leadless Chip Carrier (package)
LDO	Low-dropout Regulator
LNA	Low-noise Amplifier
MCU	Microcontroller Unit/Microprogrammed Control Unit
MSAS	Multi-functional Satellite Augmentation System (Japan)
MSL	Moisture Sensitivity Levels
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
OC	Open Connector
PCB	Printed Circuit Board

Abbreviation	Description
PI	Power Input
PMU	Power Management Unit
PSRR	Power Supply Rejection Ratio
QZSS	Quasi-zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circular Polarization
RMS	Root Mean Square
RoHS	Restriction of Hazardous Substances
RTC	Real-Time Clock
RTK	Real-Time Kinematic
RXD	Receive Data (Pin)
SAW	Surface Acoustic Wave
SBAS	Satellite-based Augmentation System
SMD	Surface Mount Device
SMT	Surface Mount Technology
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SV	Visible Satellite
TCXO	Temperature Compensated Crystal Oscillator
T_operating	Operating Temperature
TTFF	Time to First Fix
TVS	Transient Voltage Suppressor
TXD	Transmit Data (Pin)
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Abbreviation	Description
UDR	Untethered Dead Reckoning
$V_I$max	Maximum Input Voltage
$V_I$min	Minimum Input Voltage
$V_I$nom	Normal Input Voltage
V_{IH}max	High-level Maximum Input Voltage
V_{IH}min	High-level Minimum Input Voltage
V_{IL}max	Low-level Maximum Input Voltage
V_{IL}min	Low-level Minimum Input Voltage
$V_O$nom	Normal Output Voltage
V_{OL}max	Low-level Maximum Output Voltage
V_{OH}min	High-level Minimum Output Voltage
VSWR	Voltage Standing Wave Ratio
WAAS	Wide Area Augmentation System
XTAL	External Crystal Oscillator